

A photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics, and a production method

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10 The structure of a photodetector for low luminous intensities to be processed is described, in which the photo sensitive element (photocell), a transimpedance amplifier and corresponding evaluation electronic are commonly integrated in monolithic manner, wherein a vertical arrangement of the photo sensitive element and the electronic circuitry is suggested. This offers the advantage of increasing the sensitivity of the photodetector and of saving chip area (single chip solution). When mounting the
15 photodetector cost savings may be achieved, since the chip package may be designed smaller and less complex.

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20 In photo electric systems, such as opto-couplers, infrared receivers circuitry for IR remote controls, image sensors or CD/DVD photodetector ICs, various technological concepts for realization exist due to the very different requirements with respect to the "light to voltage conversion". It may be distinguished between fully integrated circuits, in which the detector (mostly a photo diode) and the associated electronic are side by side
25 combined in the chip, and two-chip approaches, in which the detector as a separate chip is connected with the amplifying and evaluating electronics via a bond wire.

Fully integrated solutions allow, among others, an immediate signal processing and thus are specifically suited for high operating speeds/data rates (e.g., CD/DVD PDICs –
30 PDICs are photodetector integrated circuits). Fully integrated systems are unavoidable when a plurality of optical signals are to be detected concurrently in a spatially very restricted neighbourhood (for example, scanner lines, image sensors, measurement tasks).

35 For applications involving low luminous intensities to be processed large detector areas are necessary. These large areas may not commonly be integrated with the signal processing circuit portions on a reasonable economic basis. The reason for this resides in the fact that due to the integrated amplifier and evaluation electronics complex and thus expensive manufacturing processes (CMOS, BiCMOS) are used. In this way for

the technologically less sophisticated large detector area (e.g., photo diode area) the same high costs caused by technology would occur. For this reason semiconductor technologies are used for the different chips in the presently existing two-chip solutions for low luminous intensities, which are optimally adapted to the requirements. However, in this way also additional cost for mounting, an increased requirement for space and thus larger packages are necessary. However, due to the electric connection of the detector chip and the signal processing IC via a bond connection an increased exposure to electromagnetic interfering radiation may occur. This especially holds true for conventional IR receiver modules for infrared remote controls, which are installed in TV devices in the vicinity of cathode ray tubes or LC displays. This may only be compensated for by complex and thus expensive packages, cf., data sheet Sharp, attachment GP1UE26RK.pdf.

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It is an object of the present invention to provide a photodetector that the disadvantages described above in view of detectors for low illumination powers to be processed according to the prior art may be overcome with respect to the monolithic integration of the evaluation electronic.

The object is solved by the features recited in claims 1, 7 or 10.

The subject-matter of claim 1 provides the advantage that the photo sensitive area of the detector may extend substantially across the entire area that corresponds to the chip area, and this area may also be used for the integration of the amplifier circuit and/or the further signal processing. The technological effort for the manufacturing is hereby slightly increased due to the vertical connection of the photo diode portion with the integrated circuit via vertically extending (parallel with respect to the normal direction of the chip) doped channels, for instance, via a modified isolation trench; the required area and other costs caused thereby for the overall system are, however, reduced in an over proportional manner. Moreover, due to the compact configuration parametric advantages are obtained compared to conventional two-chip approaches.

Advantageous embodiments of the subject-matter of claim 1 are described in the dependent claims.

In this respect a trench is particularly advantageous that is used, based on its design, as an electric connection between the photo cell and the electronic circuit.

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The invention will be explained in more detail by illustrative embodiments. The figures
5 are self-explaining and thus only require a short more detailed discussion.

Figure 1 is a schematic view of a first example of the vertical configuration of
photocells 20 and electronic circuits 30 according to the present
invention, which are electrically connected 40 by a modified trench,
10 wherein the entire arrangement is monolithically integrated.

Figure 2 is a schematic representation of a vertical integrated detector system in
a package 60, wherein the enclosing sealing material 61 is transparent
for light having the signal wavelength.

Figure 1a is a schematic representation of another embodiment of the vertical
configuration of photocells and electronic circuits according to the
present invention, which are electrically connected by a modified trench
in a monolithic manner.

Figure 2a is another schematic representation of a vertical integrated detector
system in a package, wherein the enclosing sealing material is
transparent for light having the signal wavelength.

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For manufacturing a monolithic photodetector 10 the following process flow may be
used:

30 The starting material for all embodiments is a high-ohmic silicon wafer (100 ...
1000 Ohm*cm), for instance, p-conductive. A masked (mask defined) counter-doping
process, for instance based on phosphorous ions, is performed into the wafer from one
wafer surface V. The mask may expose substantially the entire subsequent chip size.
Following an appropriate anneal process (that may be associated with an oxidation, the
35 step of which will serve as an alignment tool) an epitaxial process including the same
dopant conductivity type as included in the initial wafer is then be performed on the non-
opposing wafer surface V at a higher dopant concentration (5 ... 50 Ohm*cm) and with
a thickness in the range of 10 ... 25 µm.

By means of this epitaxial layer 28 local dopants for contacting the now buried counter-doped layer 29 are introduced, which forms the substantial portion of the photocell. This may be accomplished by a well-known Sinkers diffusion.

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In the example shown the dopant concentration is generated by etching deep isolation trenches 41 down into the buried layer 29 and subsequently doping the sidewalls 41a, 41b by a specifically tilted implantation process. Subsequently, the opening is filled with polysilicon.

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Alternatively, the isolation trenches may be filled with doped polysilicon and the previously described implantation of the sidewalls may be omitted.

Once the isolation trenches are closed and planarized, a standard CMOS or BiCMOS process is performed on the basis of this epitaxially grown wafer side. The actually buried photocell 20 is connected with the circuit 30 at the surface by means of the isolation trenches 41 or in the other example by means of the isolation trenches 40.

The layout of the circuit 30 is designed such that the contact regions 41 or 40 of the buried photocell (e.g. a diode) are immediately involved in order to realise very short conductive paths. Electric connections (40) between the photocell and the electronic circuit are provided with an extension in a direction along a perpendicular direction with respect to the chip plane (the normal direction).

After completion of the conventional semiconductor manufacturing process the entire semiconductor wafer is thinned at the side R facing away from the electronic circuit and optionally an antireflective coating (ARC) 21 is deposited on the backside R of the wafer. The chip provided after the dicing of the chip is then mounted upside down (that is, the circuit 30 facing downwardly) on a printed board (flip chip technique), such that the photocell 20 has its front side facing upwardly to be accessible. The flip chip technique is advantageous in view of an optimal utilization of the vertical integration of the detector and the circuit.

Alternatively, the chip may be formed in a conventional manner within a "clear mold package" according to a "chip on lead" technique by bond connections for the supply voltage and the output signal. In this case illumination is possible from the one side (electronic side) or the other side (detector side).

In this way the photodetector provided for processing low luminous intensities comprises monolithically integrated transimpedance amplifiers and evaluation electronics. An actual photocell portion is assigned to the one chip side. The light is preferably received from this side. Electronic circuits are provided on the opposing chip side. Electric connections are provided between the photocell and the electronic circuit(s) and have an extension along the direction perpendicular with respect to the chip plane.

The photo detection of the incident light is performed such that the light impinges onto the backside or the front side and generates, depending on the wavelength, electron/hole pairs within the first 10 μ m to 20 μ m.

These electron/hole pairs diffuse into the space charge region of the buried diode and generate there a photo voltage or a photo current, depending on the circuit configuration, the signal of which may be evaluated and processed by the overlying CMOS or BiCMOS circuit 30, which are here provided as a monolithically integrated transimpedance amplifier and an evaluation electronics.

The electric connections between the photocell portion and the electronic circuit are formed by specifically filled trenches that are doped in certain areas, wherein the specifically filled trenches comprise doped sidewalls that establish the electric connection between the photocell and the electronic circuit.

The specifically filled trenches may be filled with doped polysilicon, which provides the electric connection between the photocell and the electronic circuit, wherein the specifically filled trenches may also be used for the electrically non-conductive separation (insulation) of different chip areas.

List of reference signs

- 10 monolithically integrated (single crystalline) photodetector
- 5 20 photocell portion
- 30 electronic circuit portions
- 40 electric connections
- 10 41 conductive isolation trenches
- 60 package
- 15 61 sealing compound

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We claim:

1. A photodetector for processing low luminous intensities comprising a monolithically integrated transimpedance amplifier and evaluation electronics,
5 further comprising
an actual photocell portion (20) is associated with one chip side (R), from which preferably light (L) is incident,
an electronic circuit portion (30) is formed on the opposite chip side (V);
electric connections (40, 41) between said photocell portion (20) and the electronic
10 circuit portion (30), said electric connections extending in a direction parallel to an orthogonal direction (chip normal) with respect to the chip plane.
2. The photodetector of claim 1, wherein said electric connections between said photocell portion (20) and said electronic circuit portion (30) are formed by
15 (specifically) filled trenches (40, 41) doped in specified areas that are in particular extending in a crystalline semiconductor.
3. The photodetector of claims 1 and 2, wherein said filled trenches comprise (conductively) doped sidewalls (41a, 41b), which form the at least one electric
20 connection between said photocell portion (20) and said electronic circuit portion (30), and which particularly entirely extend through the crystalline semiconductor.
4. The photodetector of claims 1 and 2, wherein filled trenches (40, 41) are filled with doped polysilicon for establishing said electric connections between said photocell
25 portion (20) and said electronic circuit.
5. The photodetector of any claims 1 to 4, wherein said filled trenches are also used for an electrically non-conductive isolation (insulation) of different chip areas.
- 30 6. The photodetector of any claims 1 to 5, said photodetector being formed by CMOS or BiCMOS processes.

7. **A method** for forming a photodetector according to claim 1 for processing low luminous intensities, said photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics (30), the method substantially comprising the steps of:

- 5 - using high-ohmic silicon (100 to $1000 \text{ Ohm} \cdot \text{cm}$) of a first conductivity type, in particular a p-type, in a wafer as an initial material,
- forming an area of opposite conductivity type by counter-doping based on a mask, in particular by ion implantation, and subsequently annealing the wafer side (V) receiving the evaluation electronics (30);
- 10 - performing an epitaxy process for forming a layer having a thickness of substantially 10 to $25 \text{ }\mu\text{m}$ and the first conductivity type of the initial material having a doping corresponding to a range of 5 to $50 \text{ Ohm} \cdot \text{cm}$ on the one wafer side;
- contacting the counter-doped layer now being buried (according to the second
- 15 step) by locally providing a doping of the epitaxy layer by means of one of a Sinkers diffusion and (specifically) filled trenches comprising doped areas;
- planarizing at least said filled trenches of the surface of the wafer side including said epitaxy layer;
- performing one of a (standard) CMOS and BiCMOS process for forming the
- 20 integrated electronic circuit (30) on the one wafer side;
- thinning the wafer at the other side,
- in particular forming an antireflective coating above said one side;
- separating and mounting the chips and sealing the chips with a sealing
- 25 material (61) that is optically transparent in a sensitive range of said photodetector.

8. The method of claim 7, for forming a photodetector, wherein

- 30 - after separating, said chips are mounted, with said one side (detector side), on a COL (chip on lead) carrier stripe, and said chips are electrically connected by bond wires in a conventional manner.

9. The method of claim 7 for forming a photodetector, wherein

- 35 - after separating, the at least one chip is mounted with the side of the electronic circuit on a printed board or a lead frame (chip carrier stripe);
- the mounted chip (10) is sealed with a sealing material (61) that is optically transparent in a sensitivity range of said photodetector.

10. **A photodetector** for processing low luminous intensities comprising monolithically integrated transimpedance amplifiers and evaluation electronics, i.e., photocell portion and evaluation electronics (20, 30) are formed in a common single crystalline semiconductor material,
5 the buried photocell portion and the overlying electronic circuit portions being associated with the chip front side (V);
electric connections being provided as trenches (40, 41) between said photocell portion and the electronic circuit portion, said electric connections extending in a direction of the chip normal or parallel with respect thereto;
10 for allowing light to be detected to be received from the backside (R) (cf, Figure 1).
11. The monolithic photodetector of claim 10, wherein said chip back side is configured for receiving said light to be detected (cf., Figure 1).
- 15 12. The monolithic photodetector of claim 10, wherein said electric connections (20) between said photocell portion and said electronic circuit are formed by specifically filled trenches doped in specified areas that are entirely extending within said crystalline semiconductor material.
- 20 13. The monolithic photodetector of any of claims 10 to 12, wherein said filled trenches (40) entirely extending within said single crystalline semiconductor material comprise sidewalls (41a, 41b) that are doped along the entire length so as to be conductive along the entire length, which form the electric connection
25 between said photocell and said electronic circuit.
14. The monolithic photodetector of any of claims 10 to 12, wherein said specifically filled trenches (41) are filled with doped polysilicon for establishing said electric connections between said photocell and said electronic circuit.
- 30 15. The monolithic photodetector of any of claims 10 to 14, wherein said filled trenches provide for an electrically non-conductive isolation (insulation) of different chip areas.
- 35 16. The monolithic photodetector of any of claims 10 to 15, wherein said photodetector is formed by CMOS or BiCMOS processes.

17. A method for forming a photodetector for processing low luminous intensities according to claim 1, said photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics, the method being characterized by the following manufacturing steps of:

- 5 17.1) using high-ohmic silicon (100 to 1000 Ohm*cm) of a first conductivity type,
- 17.2) forming an area of opposite conductivity type by counter-doping based on a mask, preferably by ion implantation, and subsequently annealing the wafer front side (carrying the evaluation electronics in a later stage),
- 10 17.3) performing an epitaxy process for forming a layer having a thickness of 10 to 25 μm and the first conductivity type of the initial material having a doping corresponding to a range of 5 to 50 Ohm * cm at the wafer front side,
- 17.A1) contacting the counter-doped mask defined layer now being buried
- 15 (according to the step 7.2) by specifically filled trenches,
- 17.A2) planarizing said filled trenches of the wafer front side,
- 17.4) performing one of a standard CMOS and BiCMOS process for forming the integrated electronic circuit on the wafer front side,
- 17.5) thinning the semiconductor wafer from the wafer backside,
- 20 17.6) after separating the chips, mounting the chips on the printed board or a lead frame (chip carrier stripe), said front side (the side carrying said electronic circuit) facing downwardly, and sealing said chip with a sealing material that is optically transparent in the sensitivity range of said photodetector.

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18. The method of claim 17, wherein an order is determined by the continuous numbering.

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19. The method of claim 17, wherein the steps 17.A1 and the subsequent step 17.A2 are always performed after step 17.3 or alternatively after step 17.4 or within the methodology of step 17.4.

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ABSTRACT

The aim of the invention is to configure a photodetector (10) such that no disadvantages
5 are created for processing low luminous intensities on detectors known in prior art,
especially when monolithically integrating the evaluation electronics. Said aim is
achieved by a photodetector for processing low luminous intensities, comprising a
monolithically integrated transimpedance amplifier and monolithically integrated
evaluation electronics. An actual photocell component (20) is assigned to the chip face
10 onto which the light preferably falls. Electronic circuit components (30) are arranged on
the opposite chip face. Electrical connections (40) between the photocell and the
electronic circuit are provided with an extension in the direction running perpendicular to
the chip normal.

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Legend to figures:

Fig. 1a

20 photodetector
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30 evaluation electronics

wafer (chip) front side
wafer (chip) backside
10 light with $\lambda=890\text{nm} \dots 950\text{nm}$

Fig. 2a

15
light with $\lambda=890\text{nm} \dots 950\text{nm}$
chip backside
sealing material
photodetector
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